

HapsTrak II standard



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Revisions

Rev.	Date	Comment	Author
1	2007-08-28	Original version	Jonas Magnusson
2	2007-11-28	Added revision history, Fixed pin numbers in Appendix 6.1.3. added 5.2 ordering information	Jonas Magnusson
3	2008-03-10	Updated download link on page 10	Jonas Magnusson
4	2008-03-10	Updated appendixes 6.1.1 through 6.1.4	Jonas Magnusson
5	2008-06-16	Corrected 2.2. Text "B15/16," to "B17/18,"	Jonas Magnusson

This document describes the HapsTrak II standard. The HapsTrak II standard is totally backwards compatible with the previous HapsTrak I standard, also known as "HapsTrak" only. Boards compliant with HapsTrak I will not lose any functionality in HapsTrak II.

This document describes the mechanical, electrical and functional properties of HapsTrak II.

The mechanical aspects are the connector itself and the HapsTrak II standard module, which is a set of mechanical specifications concerning where to place connectors, holes, and outlines in order to comply with HapsTrak II.

The electrical aspects are the I/O banking rules, power supply, clocks and voltage reference.

The functional aspects are stacking, clocking and powering the boards.

This document states the nomenclatures used in HapsTrak II.

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1. Mechanical description

1.1 Connector

HapsTrak II is a connector and module standard for HAPS boards. The connector is based on the same QTH/QSH-060 connector pair from Samtec, Inc., which is used by HapsTrak I. However, eight extra pins have been added to the connector body, which now houses 128 pins in total. The new connector is backwards compatible with HapsTrak I. HapsTrak I daughter boards will not lose any functionality when mounted on a HapsTrak II connector, but they will not be able to benefit from the features of HapsTrak II.

At each “corner” of the connector there is a pin with an ‘H’ prefix. This indicates that it is a HapsTrak II unique pin and that it shall not be confused with older connectors. The H-pins provide greater power supply capabilities and a serial data interface to daughter boards. The new pins are placed on the same 0.5 mm spacing as the previous pins, and an old connector can very well be mounted on a new HapsTrak II footprint.

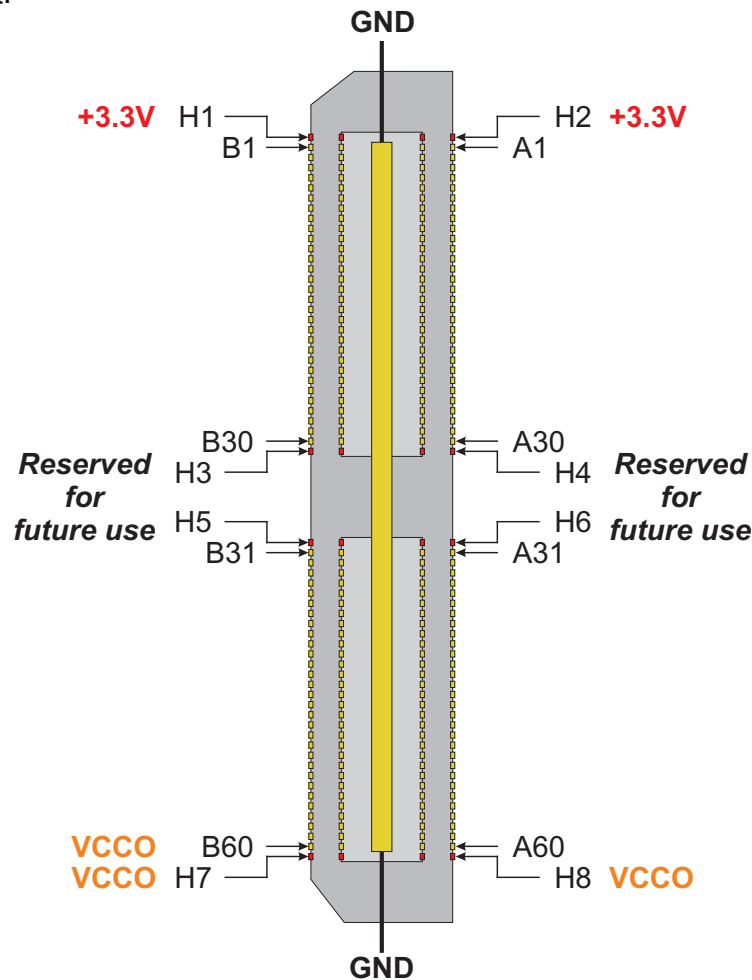


Figure 1

1.2 Module

HapsTrak II includes a maximum module size of 70x50 mm for a 1x1 module. In order to keep the stacking and cascading features of HapsTrak II, the maximum usable area in a 1x1 module is 69x49 mm leaving a 1 mm gap between modules.

On each side of the connector there must be a 3.2 mm mounting hole. Even if the module is a 1x1 module with only one connector, there must be a hole or cutout in the board outline allowing a pair of mounting posts to be screwed down.

There shall be two more 3.2 mm holes at the left edge of the module where two support stands can be attached. If a board is made up of more than one standard module (e.g. a 2x3 board), the holes for support stands can be left out between two connectors since they are not meaningful there. Notice that the holes for support stands should not be confused with the holes for mounting posts.

The top side connector must always be a QTH type connector whereas the bottom side connector shall always be a QSH type. The QTH and QSH connectors should be placed in such a way that they sit right on top of each other. The indentation on the connectors should both be pointing to the left according to the picture. See section 4 for detailed layout information.

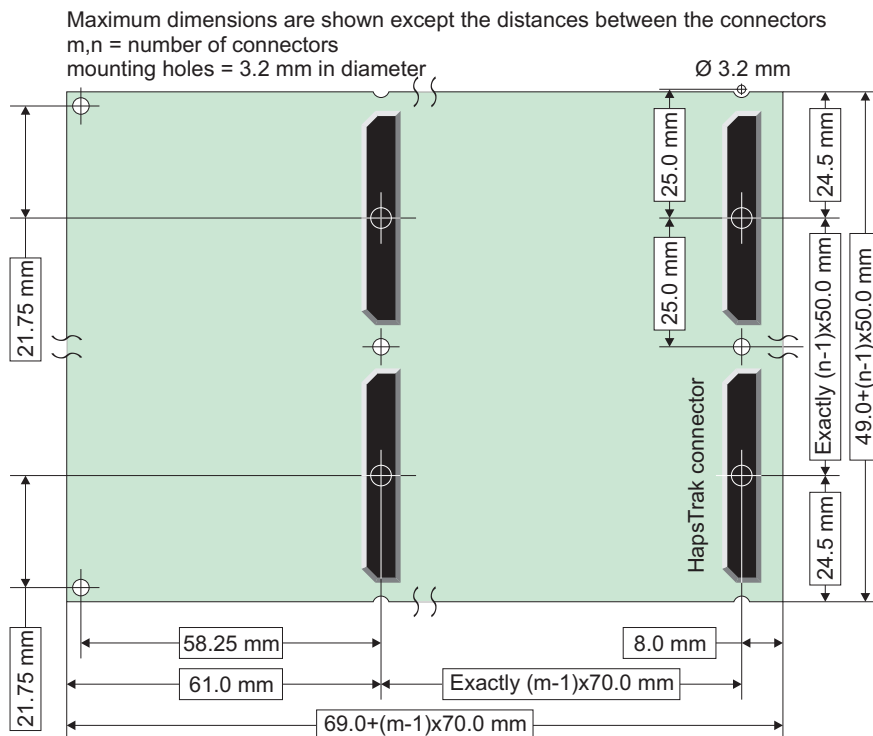


Figure 2

2 Electrical description

2.1 I/O bank rules

The HapsTrak II standard includes a defined way to interface to Xilinx FPGAs. HapsTrak II guarantees neighborhood in silicon, thus making timing closure easier to achieve especially when dealing with source synchronous buses. Using HapsTrak II, each of the 4 regions in the connector contains pins that are adjacent both in the connector and in the FPGA.

HapsTrak II states that I/O banks are adjacent and the lowest I/O bank (numbered 1 in figure 3) shall start from pin B59 and end with pin B33. The next I/O bank (numbered 2 in figure 3) must be adjacent to the first and start with pin B32 and end with pin B1. Two more I/O banks are connected to the right (A-side) of the connector

2.2 Clock Capable pins

Some pins are called CLKN or CLKP and are local clock pins, referred to as “clock capable” in Xilinx documentation. In Virtex™-4 and Virtex™-5, these pins can drive local clock trees and are specialized to be used as memory strobes or local clocks. Positions A15/16, A31/32, A47/48, A59/60, B1/2, B17/18, B33/34, B49/50 are such clock capable pins.

2.3 P/N pairs

Almost all pins in a HapsTrak II connector are capable of LVDS operation¹, therefore it becomes necessary to state whether a pin is negative (N) or positive (P).

HapsTrak II states that odd number pins must be negative and even number pins must be positive. The lowest numbering pin in a LVDS pair is the N-pin.

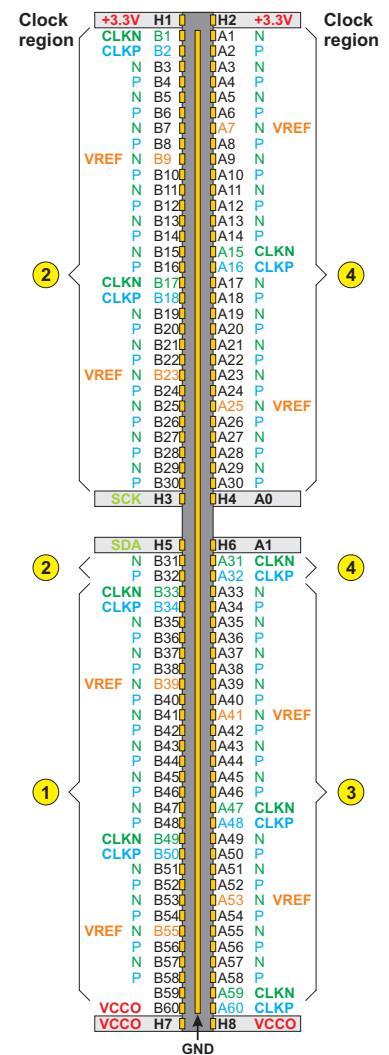


Figure 3

¹ Notice that CC pins on Virtex-4 may not be used to drive LVDS signals, although they are capable of receiving LVDS signals. Pin B59 is not a LVDS compatible pin since it lacks a P-pin to pair up with.

2.4 Power supply pins

HapsTrak II defines two power supply rails in each connector, 3.3 V and VCCO. It is not allowed to connect two power rails (neither 3.3 V nor VCCO) between two connectors on the same daughter board. On motherboards, several connectors can share a power rail since they by default never pass the voltage on downwards.

2.4.1 3.3V rail

Pins H1 and H2 are reserved for the 3.3 V supply. This supply is an auxiliary supply to daughter boards and has nothing to do with the I/O standard used in the FPGA. This power supply should be connected to the QTH H1 and H2 pins on motherboards. On daughter boards, the QSH H1 and H2 pins should be connected to the QTH H1 and H2 pins.

2.4.2 VCCO rail

Pins B60, H7 and H8 are connected to VCCO, the I/O voltage supply to the FPGA on a motherboard. This power supply should be connected to the QTH H7 and H8 pins on motherboards. On daughter boards the QSH H7 and H7 pins should be connected to the QTH H7 and H8 pins.

2.4.3 Vref pins

Each HapsTrak II connector has voltage reference pins on positions A7, A25, A41, A53, B9, B23, B39, B55. The voltage reference pins are multi purpose pins and are used as regular I/O unless certain I/O standards are used, such as SSTL. Then these pins become voltage reference pins. See the Virtex™-5 user guide at <http://direct.xilinx.com/bvdocs/userguides/ug190.pdf> for further information regarding the Vref pins.

2.5 RFU pins

Pins H3 through H6 are reserved for future use and should not be connected as of yet.

3 Functional description

3.1 Clock regions

Virtex™-5 FPGAs have global clock trees and local clock trees. Clock Capable (CC) pins can directly clock local clock trees but not global clock trees. Local clock trees can clock the indigenous I/O bank and the direct neighboring I/O banks. This will affect HapsTrak II connectors since they contain 4 I/O banks, thus a local clock tree can not clock all of the I/O's in a connector. Figure 4 shows how the clock regions are connected in a motherboard using HapsTrak II, for instance HAPS-54. The three connectors are adjacent not only physically on the board and in the FPGA chip, but also have adjacent clock trees. For instance, I/O bank 2 in the lowest connector can clock its neighboring I/O banks 1 and 3. I/O Bank 4 in the same connector can clock its neighbor in the connector I/O bank 3, but also I/O bank 1 in the above connector.

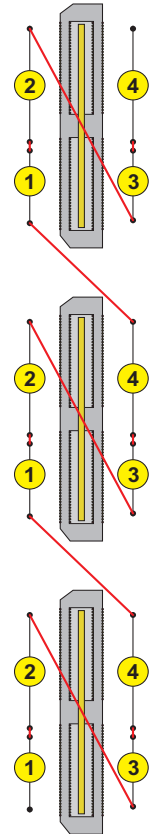


Figure 4

3.2 Stacking

One of the benefits of HapsTrak II is the expandability and flexibility that it provides. When HapsTrak II boards are stacked, there are several issues that must be heeded.

Maximum component height on the bottom side is 3mm. All boards should leave 3 mm clearance upwards for components placed on the bottom of the next board in a stack. On a board carrying 19 mm connectors, 16 mm of component height is available.

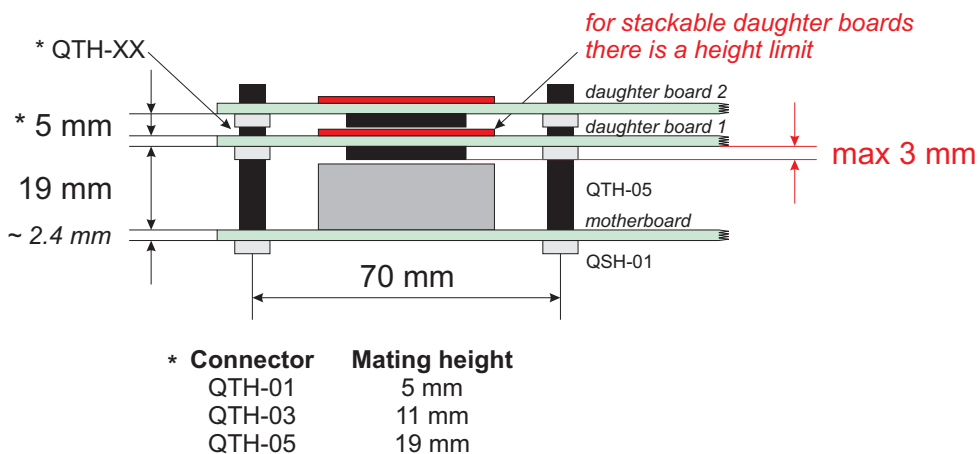


Figure 5

3.3 Power supply

Any board carrying a voltage source is prohibited by section 2.4 from passing its voltage downwards in a board stack. However, boards are required to pass on the voltage upwards. It is useful if boards have a zero ohm resistor that can be mounted or dismounted in order to break these rules. This may be used in special cases, then the lowest board in the stack need to pass on the voltage upwards in the stack in order to power the next board's VCCO.

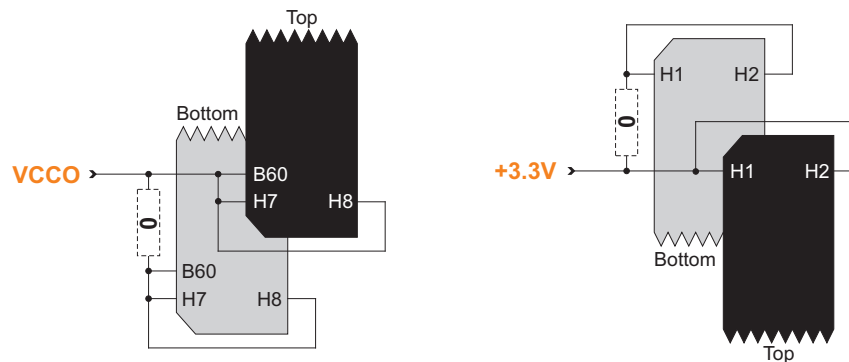


Figure 6

No pin in a HapsTrak II connector can carry more than ~1 A of current. This puts an effective limit on the VCCO power supply to ~3 A and on the 3.3 V supply to ~2 A. These currents must not be exceeded.

4 Nomenclatures

Naming conventions used in HapsTrak II are different depending on if the board is a motherboard or a daughter board.

4.1 Motherboards

Motherboards have FPGAs and connectors in a pattern according to the HapsTrak II module matrix. QTH-connectors connected to an FPGA have names that start with the FPGA letter to which the connector belongs, and then the connector number. The number starts at the lower left and increase row wise to the right according to figure 7. QSH connectors are named exactly like the QTH connector. Motherboards can have extra connectors outside the module grid, but with lower height. These can be named with a higher number. E.g., if FPGA B has a 7th connector it can be called B7 but not C7 or B4.

4.2 Daughter boards

Daughter boards follow the same numbering scheme as motherboards, but the names differ in that no FPGA letter is present. The QTH connectors on a HapsTrak II compliant daughter board should have names that start with the letter J and then a number according to figure 7. The QSH connectors have the same number as the QTH connector on top of it, but with an X between the letter J and the number. For instance on a 1x1 module daughter board, the QTH connector must be called J1 and the QSH connector must be called JX1.

$J(((m-1)*n)+1)$	$J(((m-1)*n)+2)$.	.	.	$J(M*N)$
.
.
.
$J(N+1)$	$J(N+2)$.	.	.	$J(2n)$
J1	J2	.	.	.	JN

Figure 7

5 Other resources

5.1 PCB templates

PCB templates for designing with HapsTrak II are available from http://www.synplicity.com/haps_supportnet/customers/cd/pcb_templates/Mentor_Expedition.zip. These templates are in Mentor Expedition format. At this point HapsTrak II is not supported for other PCB layout tools. Please contact your local PCB layout tool vendor for information on how to convert to your current design environment.

5.2 HapsTrak II connector ordering information

CONNECTOR	SAMTEC ASP	HEIGHT(Mated with QSH)	HAPSTRAK I	FOOTPRINT
QTH-01	ASP-132422-01	5mm	QTH-060-01-L-D-A	QTH
QTH-03	ASP-132424-01	11mm	QTH-060-03-L-D-A	QTH
QTH-05	ASP-125521-03	19mm	QTH-060-05-L-D-A	QTH
QSH-01	ASP-125516-03		QSH-060-01-L-D-A	QSH

6. Appendices

6.1 Mechanical drawings

6.1.1 ASP-132422-01

NOTES:
 1. POSITION QTH IS NON-STANDARD.
 2. USE ASP-132422-01-8 BODY.
 3. (C) REPRESENTS A CRITICAL DIMENSION.
 4. MINIMUM GROUND PLANE RETENTION: 1 LB.
 5. MINIMUM GROUND PLANE RETENTION: 1 LB.
 6. PARTS TO BE MOLDED TO POSITION.
 7. INDEPENDENT OF THE GROUND OR SIGNAL PINS RESPECTIVELY.
 8. GROUND PLANE PRESS-HIGHT MUST BE .0031 (.071) LESS THAN THE MAXIMUM HEIGHT.
 9. PART TO BE PACKAGED IN TRAYS.

SECTION "A-A"

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PROPRIETARY NOTE
 UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES ARE:
 .XX: ± 0.01 (3)
 .XXX: ± 0.005 (15)
 .XXXX: ± 0.0005 (51)
 DO NOT SCALE DRAWING

DESCRIPTION:
 MODIFIED QTH ASSEMBLY
ASP-132422-01

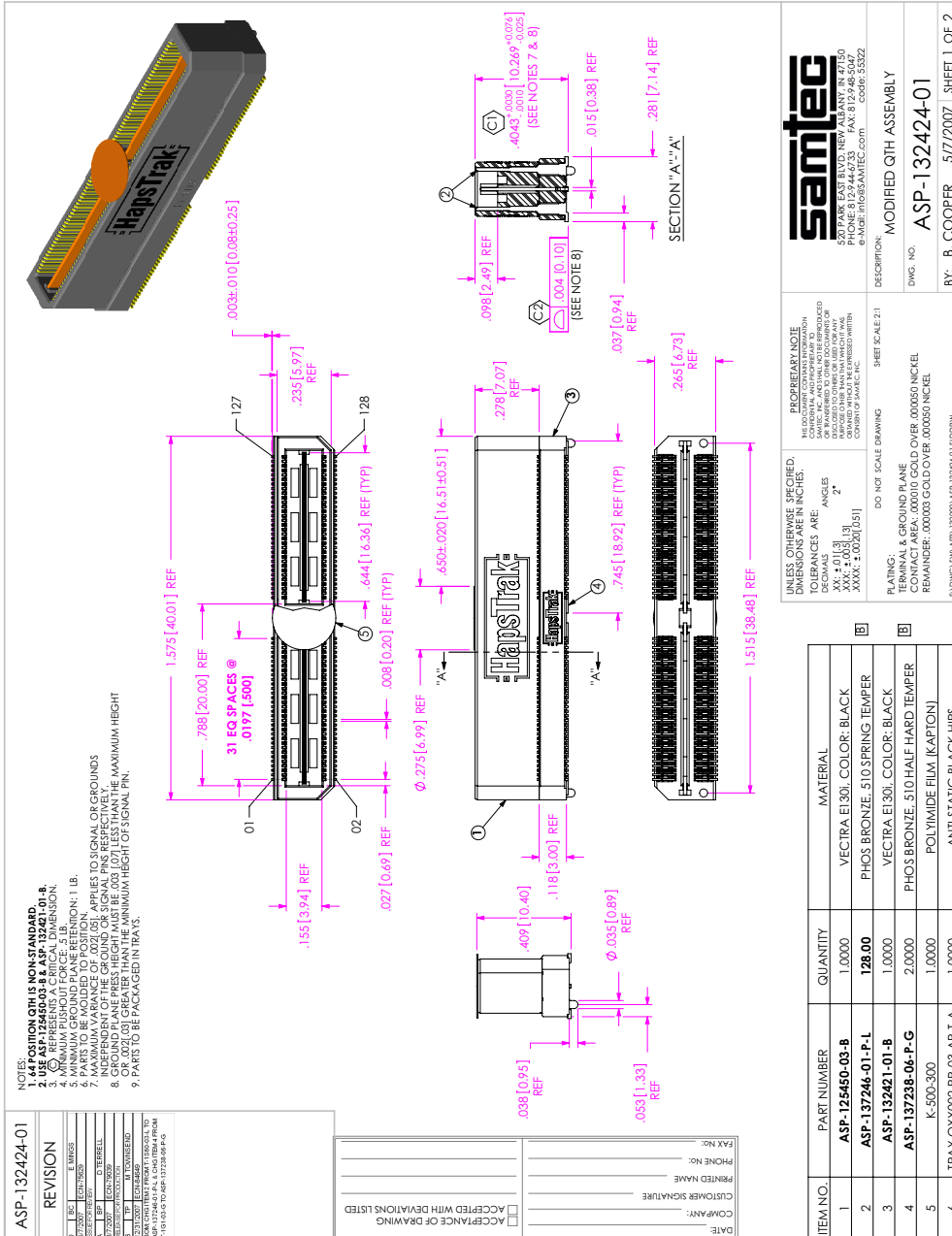
DATE: _____
COMPANY: _____
CUSTOMER SIGNATURE: _____
PRINTED NAME: _____
PHONE NO.: _____
FAX NO.: _____

ITEM NO.	PART NUMBER	QUANTITY	MATERIAL
1	ASP-132422-01-B	1,000	VECTRA EL301, COLOR: BLACK
2	ASP-137237-02-P-L	128.00	PHOS BRONZE- 510 SPRING TEMPER
3	ASP-137238-02-P-G	2,000	PHOS BRONZE- 510 HALF HARD TEMPER
4	K-500-300	1,000	POLYIMIDE FILM (KAPTON)
5	TRAY-QXXX002-PR-01-AP-T-A	1,000	ANTI-STATIC BLACK HIPS

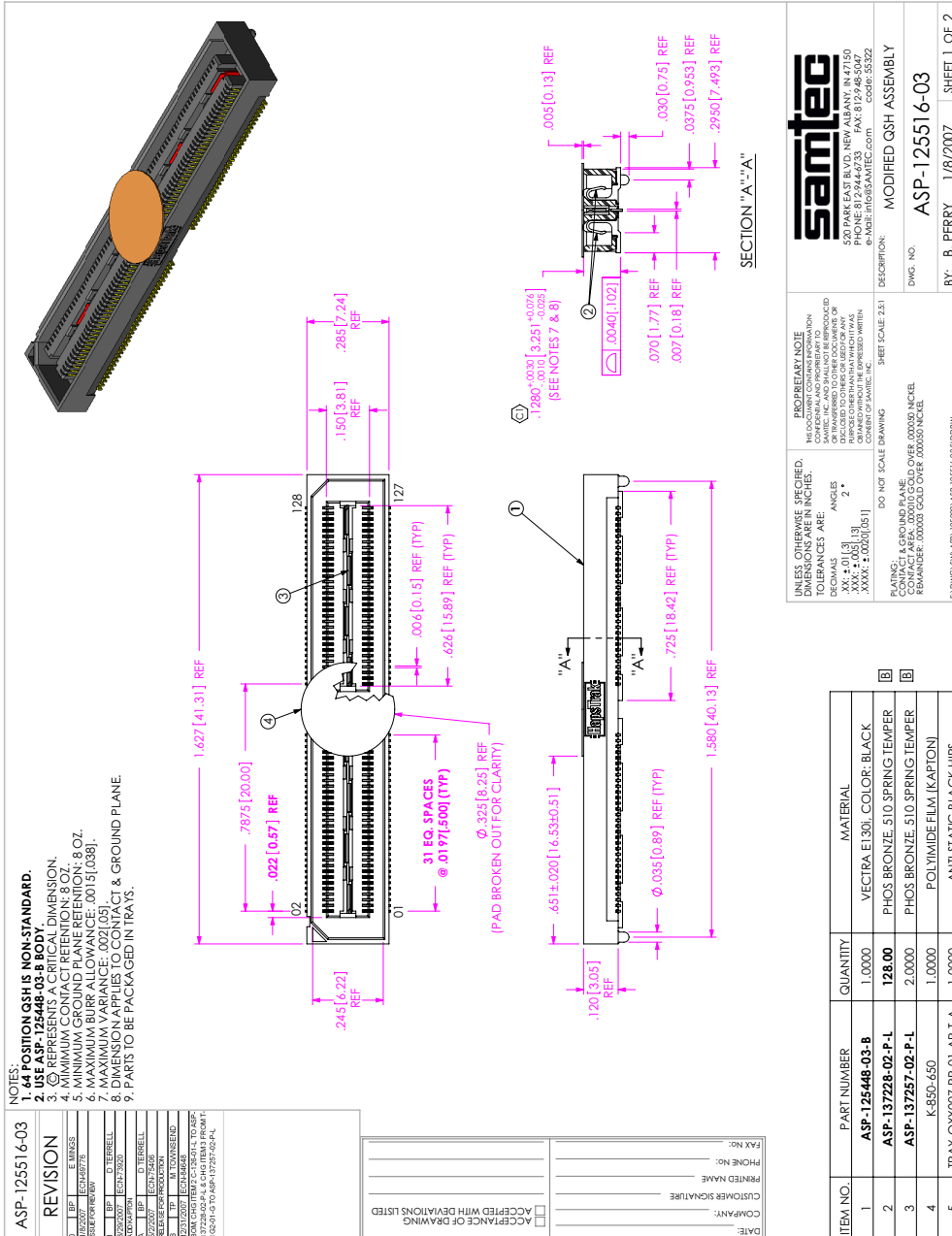
REVISED

DATE: _____
 BY: _____
 CHECKED BY: _____
 DESIGNED BY: _____
 DRAWN BY: _____
 TITLE: _____
 PART NO.: _____
 REV: _____
 QTY: _____
 ASP-132422-01-8 ITEM 8 FROM 1101
 0115 TO ASP-132422-01-P-G

6.1.2 ASP-132424-01

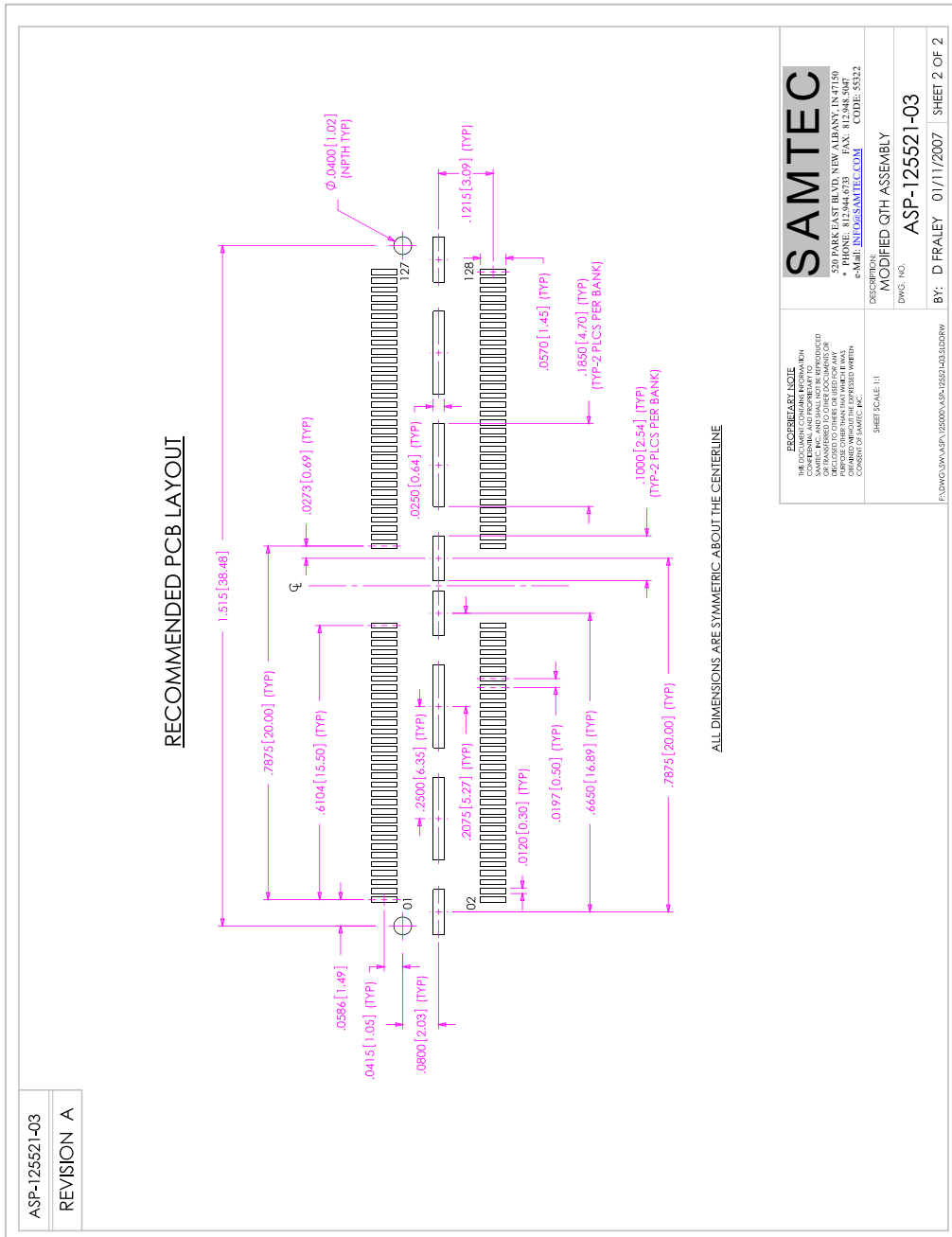


6.1.4 ASP-125516-03

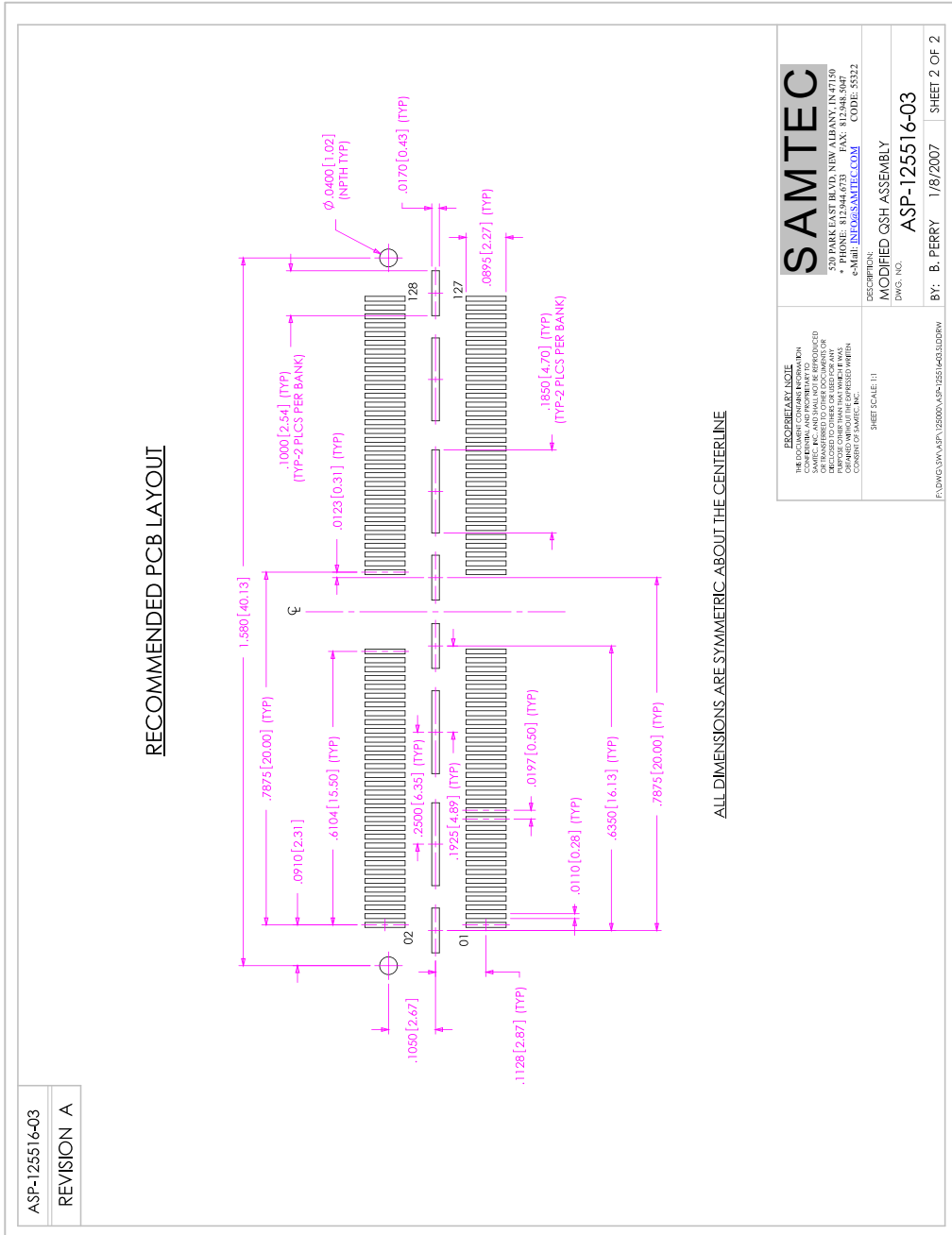


6.2 PCB footprints

6.2.1 QTH



6.2.2 QSH





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